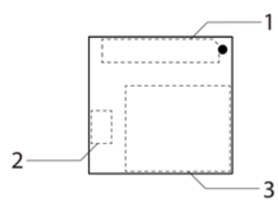
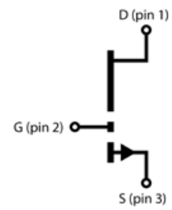
Features

- 100V enhancement mode power switch
- Bottom-side cooled configuration
- $R_{DS(on)}$ = 15 mΩ
- $I_{DS(max)}$ = 45 A
- Ultra-low FOM Island Technology® die
- Low inductance GaN*PX*® package
- Easy gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- Very high switching frequency (f > 100 MHz)
- Fast and controllable fall and rise times
- Reverse current capability
- Zero reverse recovery loss
- Small 4.6 x 4.4 mm² PCB footprint
- RoHS 6 compliant

Package Outline



Circuit Symbol



Applications

- High efficiency power conversion
- High density power conversion
- Enterprise and Networking Power
- ZVS Phase Shifted Full Bridge
- Half Bridge topologies
- Synchronous Buck or Boost
- Uninterruptable Power Supplies
- Industrial Motor Drives
- Solar Power
- Fast Battery Charging
- Class D Audio amplifiers
- Smart Home

Description

The GS61004B is an enhancement mode GaN-on-Silicon power transistor. The properties of GaN allow for high current, high voltage breakdown, high switching frequency and high temperature operation. GaN Systems implements patented **Island Technology®** cell layout for high-current die performance & yield. **GaN*PX*®** packaging enables low inductance & low thermal resistance in a small package. The GS61004B is a bottom-cooled transistor that offer very low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

Absolute Maximum Ratings (T_{case} = 25 °C except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	-55 to +150	°C
Storage Temperature Range	T_S	-55 to +150	°C
Drain-to-Source Voltage	V_{DS}	100	V
Transient Drain to Source Voltage (note 1)	$V_{DS(transient)}$	130	V
Gate-to-Source Voltage	V_{GS}	-10 to +7	V
Gate-to-Source Voltage - transient (note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current (T_{case}=25 °C) (note 2)	I_{DS}	45	A
Continuous Drain Current (T_{case}=100 °C) (note 2)	I_{DS}	35	A
Pulse Drain Current (Pulse width 100 µs)	$I_{DS\ Pulse}$	85	A

(1) For 1 µs

(2) Limited by saturation

Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\Theta JC}$	1.1	°C /W
Thermal Resistance (junction-to-top)	$R_{\theta JT}$	22	°C /W
Thermal Resistance (junction-to-ambient) (note 3)	$R_{\Theta JA}$	28	°C /W
Maximum Soldering Temperature (MSL3 rated)	T_{SOLD}	260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal vias under the thermal pad are 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm^2 each. The PCB is mounted in horizontal position without air stream cooling.

Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS61004B-TR	GaN*PX*® bottom cooled	Tape-and-Reel	3000	13″ (330mm)	16mm
GS61004B-MR	GaN*PX*® bottom cooled	Mini-Reel	250	7″ (180mm)	16mm

Electrical Characteristics (Typical values at T_J = 25 °C, V_{GS} = 6 V unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	BV_{DS}		100		V	V_{GS} = 0V, I_{DSS} = 50 µA
Drain-to-Source On Resistance	$R_{DS(on)}$		15	20	mΩ	V_{GS} = 6V, T_J = 25 °C I_{DS} = 13.5 A
Drain-to-Source On Resistance	$R_{DS(on)}$		39		mΩ	V_{GS} = 6 V, T_J = 150 °C I_{DS} = 13.5 A
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.3		V	V_{DS} = V_{GS}, I_D = 7 mA
Gate-to-Source Current	I_{GS}		100		µA	V_{GS} = 6 V, V_{DS} = 0 V
Gate Plateau Voltage	V_{plat}		3		V	V_{DS} = 80 V, I_D = 45 A
Drain-to-Source Leakage Current	I_{DSS}		0.3		µA	V_{DS} =100 V, V_{GS} = 0 V $T_{J\,=}$ 25°C
Drain-to-Source Leakage Current	I_{DSS}		50		µA	V_{DS} = 100 V, V_{GS} = 0 V T_J = 150 °C
Internal Gate Resistance	R_G		0.92		Ω	f = 1 MHz, open drain
Input Capacitance	C_{ISS}		295		pF	V_{DS} = 50 V V_{GS} = 0 V f = 1 MHz
Output Capacitance	C_{OSS}		140		pF	
Reverse Transfer Capacitance	C_{RSS}		6.2		pF	
Effective Output Capacitance Energy Related (Note 4)	$C_{O(ER)}$		276		pF	V_{GS} = 0 V V_{DS} = 0 to 50 V
Effective Output Capacitance Time Related (Note 5)	$C_{O(TR)}$		217		pF	
Total Gate Charge	Q_G		6.2		nC	V_{GS} = 0 to 6 V V_{DS} = 50 V I_{DS}= 45 A
Gate-to-Source Charge	Q_{GS}		2.4		nC	
Gate threshold charge	$Q_{G(th)}$		1.0		nC	
Gate switching charge	$Q_{G(sw)}$		2.0		nC	
Gate-to-Drain Charge	Q_{GD}		0.9		nC	
Output Charge	Q_{OSS}		11.5		nC	V_{GS} = 0 V, V_{DS} = 50 V
Reverse Recovery Charge	Q_{RR}		0		nC	

(4) $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

(5) $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}

Electrical Performance Graphs

GS61004B I_{DS} vs. V_{DS} Characteristic

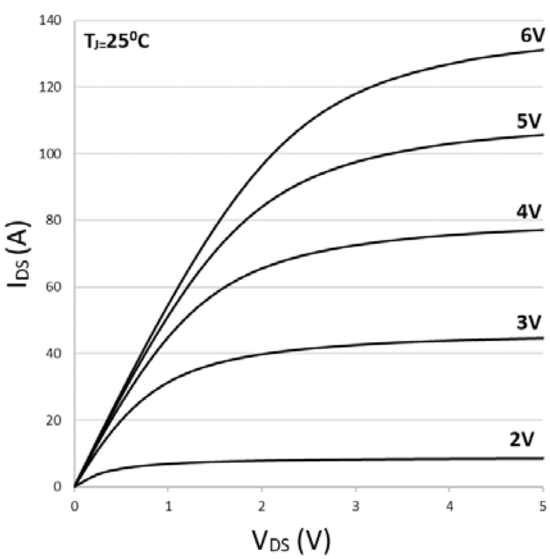


Figure 1: Typical I_{DS} vs. V_{DS} @ T_J = 25 °C

GS61004B I_{DS} vs. V_{DS} Characteristic

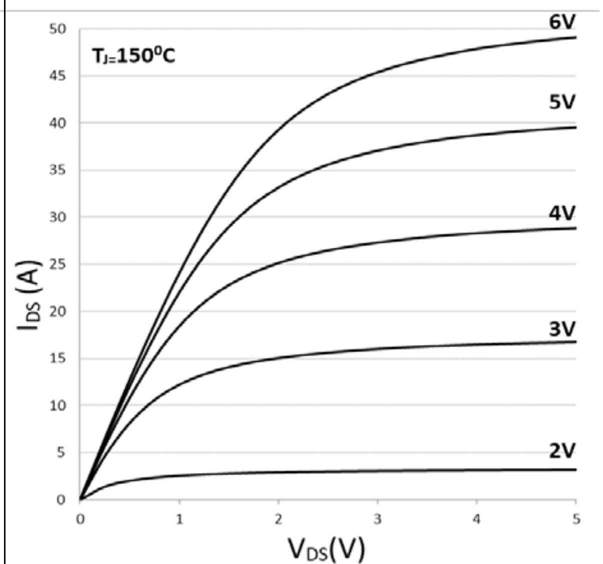


Figure 2: Typical I_{DS} vs. V_{DS} @ T_J = 150 °C

$R_{DS(on)}$ vs. I_{DS} Characteristic

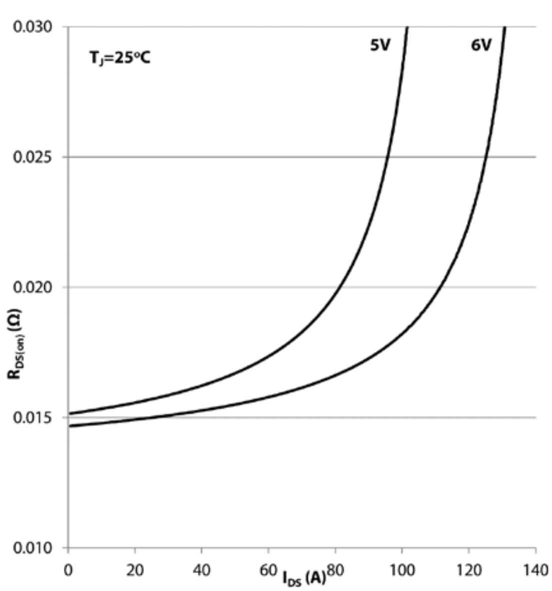


Figure 3: $R_{DS(on)}$ vs. I_{DS} at T_J = 25 °C

$R_{DS(on)}$ vs. I_{DS} Characteristic

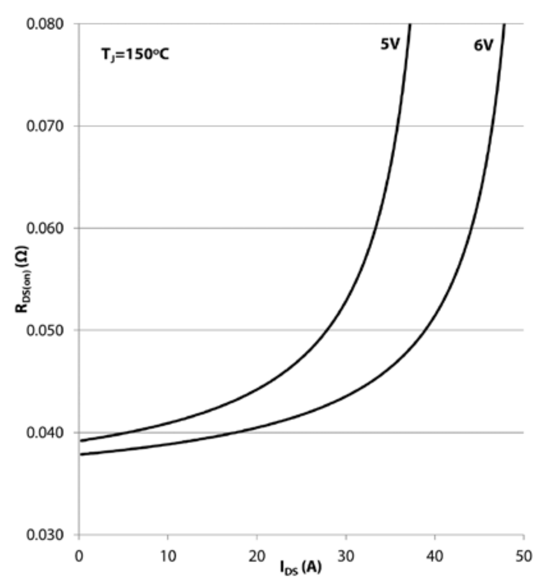


Figure 4: $R_{DS(on)}$ vs. I_{DS} at T_J = 150 °C

Electrical Performance Graphs

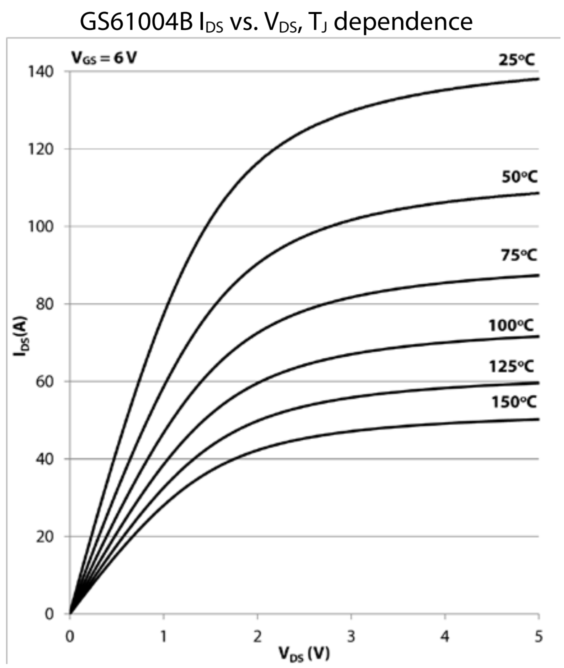


Figure 5: Typical I_{DS} vs. V_{DS} @ V_{GS} = 6 V

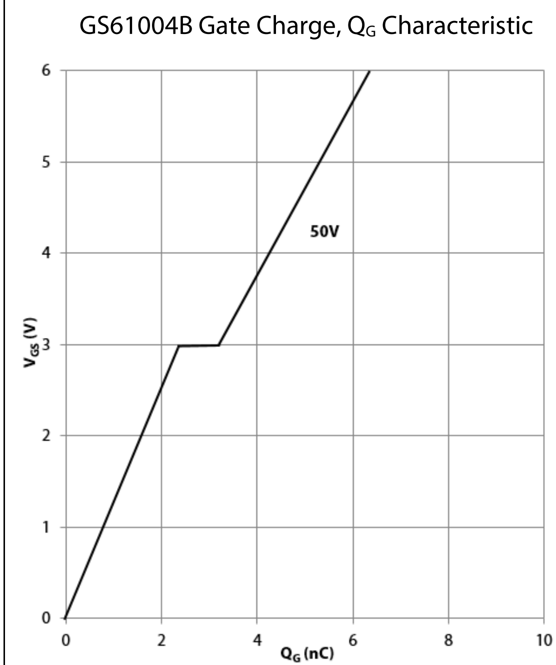


Figure 6: Typical V_{GS} vs. Q_G

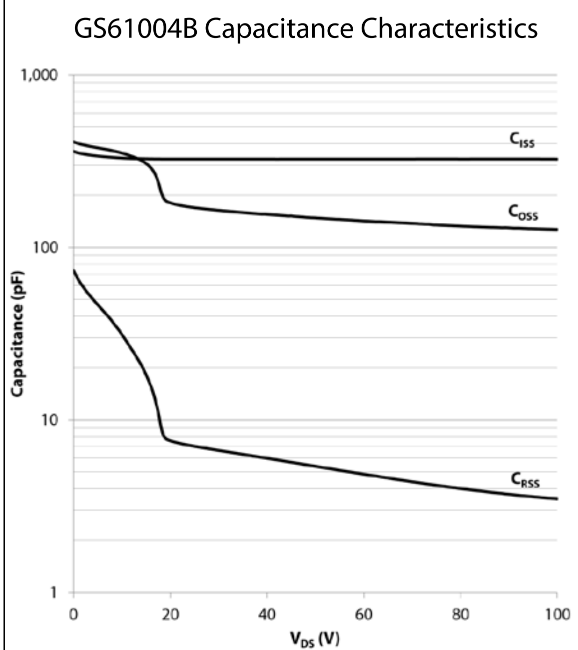


Figure 7: Typical C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

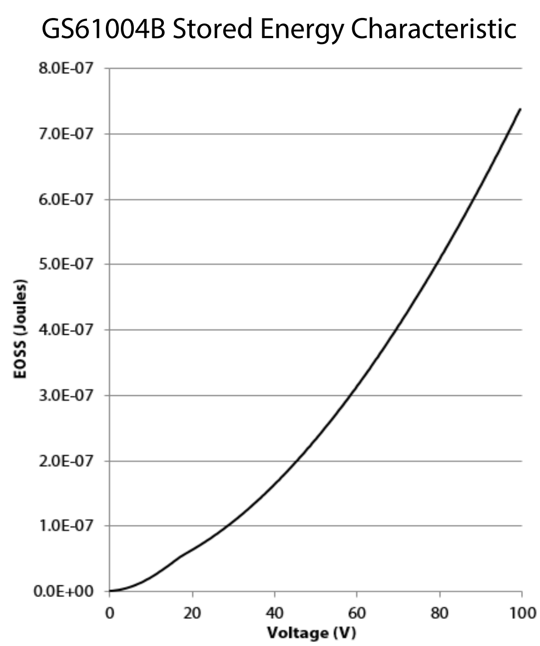


Figure 8: Typical C_{OSS} Stored Energy

Electrical Performance Graphs

GS61004B Reverse Conduction Characteristics

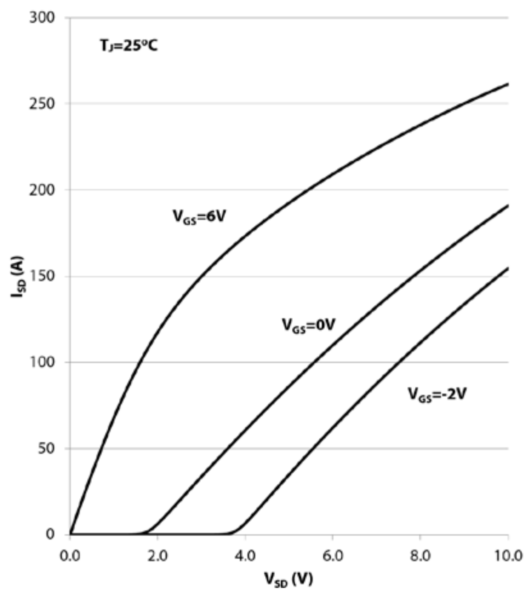


Figure 9: Typical I_{SD} vs. V_{SD}

GS61004B I_{DS} vs. V_{GS} Characteristic

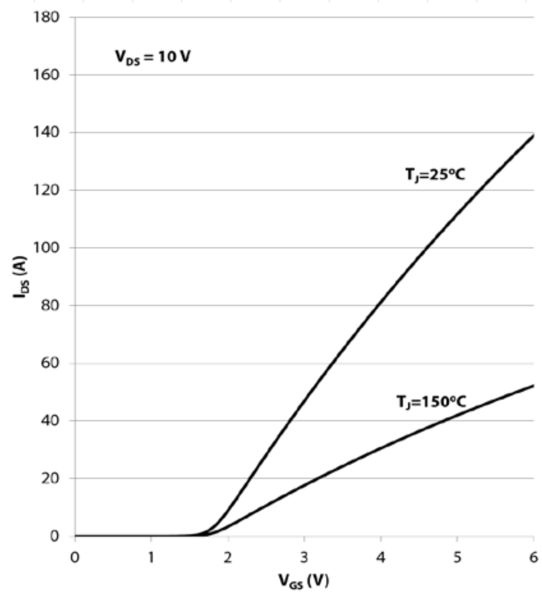


Figure 10: Typical I_{DS} vs. V_{GS}

$R_{DS(on)}$ Temperature Dependence

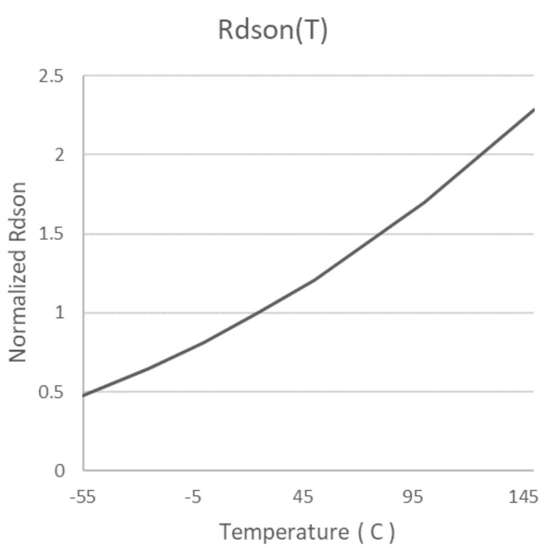


Figure 11: Normalized $R_{DS(on)}$ as a function of T_J

GS61004B IDS-VDS SOA

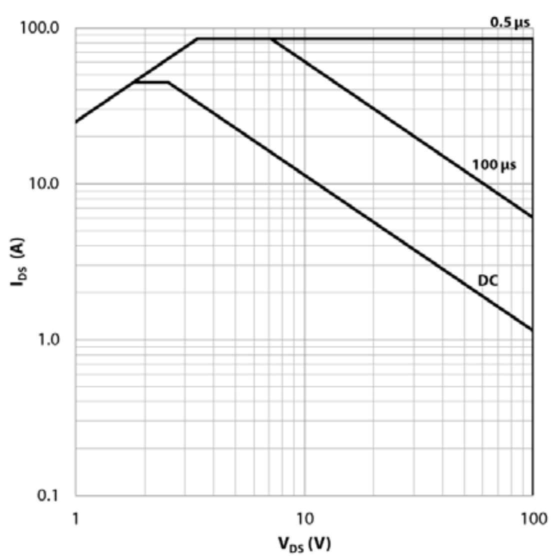


Figure 12: Safe Operating Area @ Tcase = 25 °C

Thermal Performance Graphs

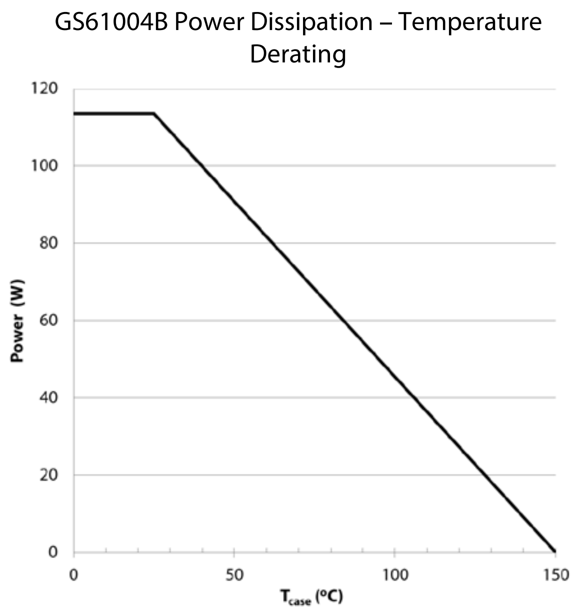


Figure 13: Derating vs. Case Temperature

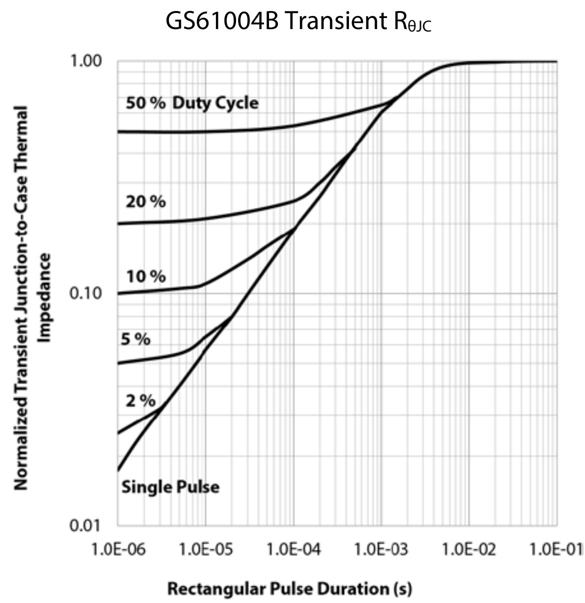


Figure 14: Transient Thermal Impedance
1.00 = Nominal DC thermal impedance

Application Information

Gate Drive

The recommended gate drive voltage is 0 V to + 6 V for optimal $R_{DS(on)}$ performance and long life. The absolute maximum gate to source voltage rating is specified to be +7.0 V maximum DC. The gate drive can survive transients up to +10 V and – 20 V for pulses up to 1 µs. These specifications allow designers to easily use 6.0 V or even 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss. For more details, please refer to the gate driver application note "GN001 How to Drive GaN Enhancement Mode Power Switching Transistors" at www.gansystems.com.

Similar to a silicon MOSFET, the external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance, $R_{G(OFF)}$ is recommended for better immunity to cross conduction. Please see the gate driver application note (GN001) for more details.

A standard MOSFET driver can be used as long as it supports 6V for gate drive and the UVLO is suitable for 6V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower Q_G when compared to equally sized $R_{DS(on)}$ MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Many non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive for GaN enhancement mode HEMT due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive will not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Alternatively, isolated drivers can be used for a high side device. Please see the gate driver application note (GN001) for more details.

Parallel Operation

Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

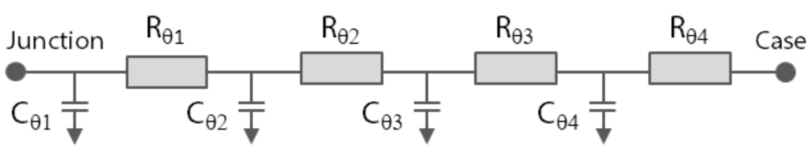
GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2 Ω) on each gate is strongly recommended to minimize the gate parasitic oscillation.

Source Sensing
Although the GS61004B does not have a dedicated source sense pin, the GaN*PX*® packaging utilizes no wire bonds so the source connection is already very low inductance. By simply using a dedicated "source sense" connection with a PCB trace from the gate driver output ground to the Source pad in a kelvin configuration with respect to the gate drive signal, the function can easily be implemented. It is recommended to implement a "source sense" connection to improve drive performance.

Thermal
The substrate is internally connected to the thermal pad and to the source pad on the bottom side of the GS61004B. The transistor is designed to be cooled using the printed circuit board.

Thermal Modeling
RC thermal models are available for customers that wish to perform detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra R_θ and C_θ to simulate the Thermal Interface Material (TIM) or Heatsink.

GS61004B RC thermal model:



RC breakdown of $R_{\Theta JC}$

R_θ (°C/W)	C_θ (W·s/°C)
$R_{\theta 1}$ = 0.035	$C_{\theta 1}$ = 3.5E-05
$R_{\theta 2}$ = 0.51	$C_{\theta 2}$ = 3.4E-04
$R_{\theta 3}$ = 0.52	$C_{\theta 3}$ = 2.9E-03
$R_{\theta 4}$ = 0.035	$C_{\theta 4}$ = 9.0E-04

For more detail, please refer to Application Note GN007 "Modeling Thermal Behavior of GaN Systems' GaN*PX*™ Using RC Thermal SPICE Models" available at www.gansystems.com

Reverse Conduction
GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition (V_{GS} = +6 V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance, $R_{DS(on)}$, similar to forward conduction operation.

Off-state condition ($V_{GS} \leq 0$ V): The reverse characteristics in the off-sate are different from silicon MOSFET as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain, (V_{GD}) exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher V_F and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than $V_{GS(th)}$+$V_{GS(off)}$ in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop "V_F" and hence increase the reverse conduction loss.

Blocking Voltage

The blocking voltage rating, BV_{DS}, is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30% higher than the rated BV_{DS}. As a general practice, the maximum drain voltage should be de-rated in a similar manner as silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The absolute maximum drain-to-source rating is 100 V and doesn't change with negative gate voltage.

Packaging and Soldering

The package material is high temperature epoxy-based PCB material which is similar to FR4 but has a higher temperature rating, thus allowing the GS61004B to be specified to 150 °C. The device can handle at least 3 reflow cycles.

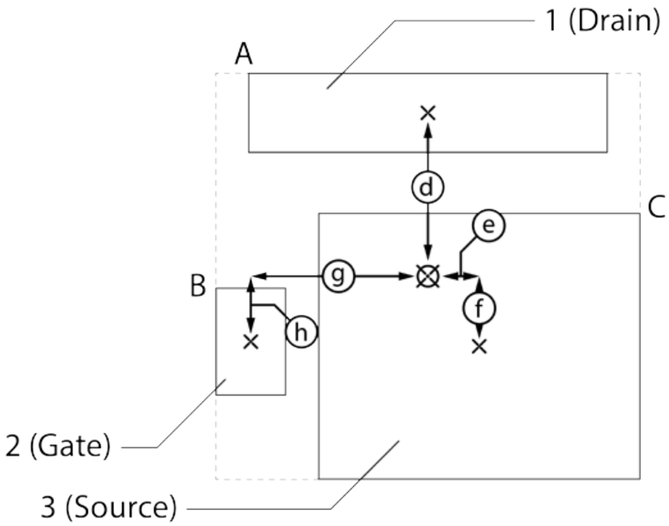
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60-120 seconds. T_{min} = 150 °C, T_{max} = 200 °C.
- Reflow: Ramp up rate 3°C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "Non-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "Non-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "Non-Clean" paste residues.

Recommended PCB Footprint for GS61004B



Pad sizes

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
A	3.85	0.85	0.152	0.033
B	0.75	1.15	0.030	0.045
C	3.45	2.85	0.136	0.112

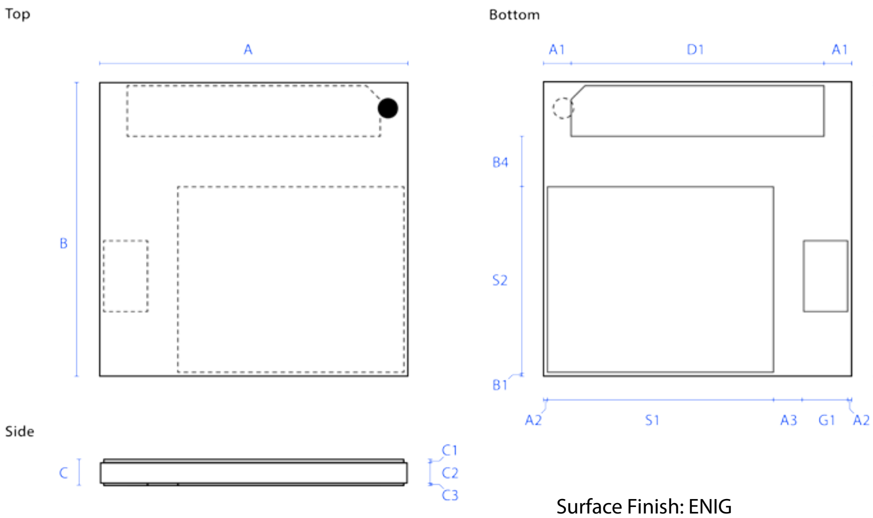
Dimensions

	mm	Inches
d	1.75	0.069
e	0.55	0.022
f	0.75	0.030
g	1.90	0.075
h	0.70	0.028

PCB pad opennings

Package outline

Package Dimensions

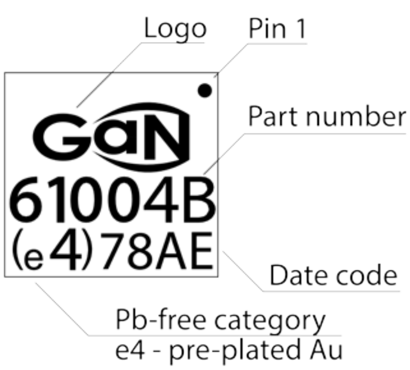


	mm	Inches	
A	4.60	0.181	± 0.10 mm (0.004")
A1	0.425	0.017	± 0.05 mm (0.002")
A2	0.075	0.003	± 0.05 mm (0.002")
A3	0.45	0.018	
B	4.40	0.173	± 0.10 mm (0.004")
B1	0.075	0.003	± 0.05 mm (0.002")
B2	1.55	0.061	
B3	0.975	0.038	± 0.05 mm (0.002")
B4	0.75	0.030	
C	0.51	0.0201	± 0.05 mm (0.002")
C1	0.045	0.0018	
C2	0.45	0.0177	
C3	0.015	0.0006	
D1	3.75	0.148	
D2	0.75	0.030	
G1	0.65	0.026	
G2	1.05	0.041	
S1	3.35	0.132	
S2	2.75	0.108	

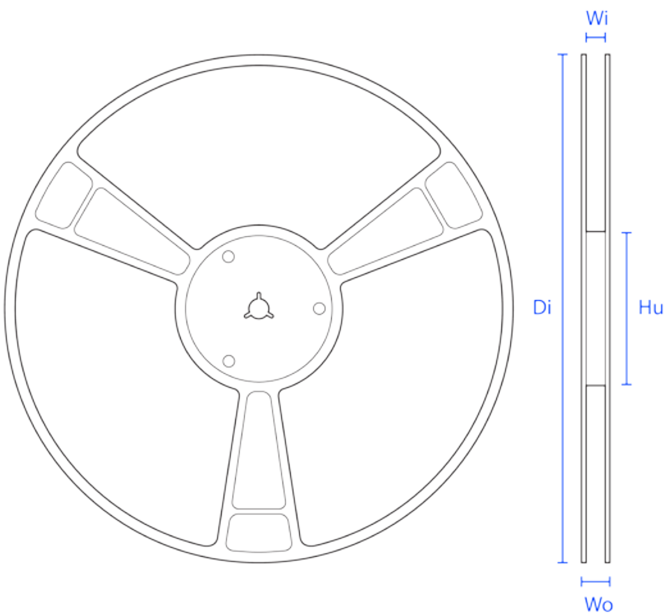
Note: Inch measurements are approximate values

Surface Finish: ENIG
Ni: 4.5 µm +/- 1.5 µm
Au: 0.09 µm +/- 0.03 µm

GaN*PX*® Part Marking

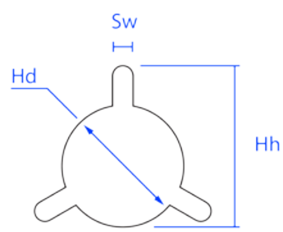


GS61004B GaN*PX*® Tape and Reel Information

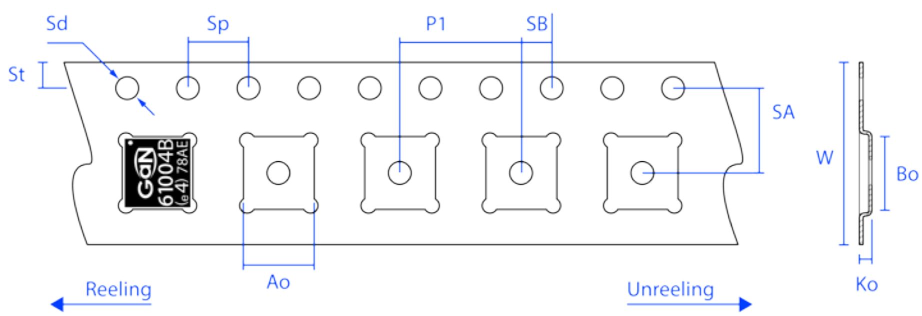


Dimensions (mm)

	13″ reel (330 mm)		7″ mini-reel (180 mm)	
	Nominal	Tolerance	Nominal	Tolerance
Di	330.0	+/- 1.5	180.0	+/- 1.5
Wo	18.4	MAX	18.4	MAX
Wi	12.4	+ 2.0 / - 0.0	12.4	+ 2.0 / - 0.0
Hu	100.0	+/- 1.5	62.0	+/- 0.5
Hh	17.2	+/- 0.2	17.3	+/- 0.2
Sw	2.2	+/- 0.2	2.3	+/- 0.2
Hd	13.0	+ 0.5 / - 0.2	13.0	+ 0.3 / - 0.2



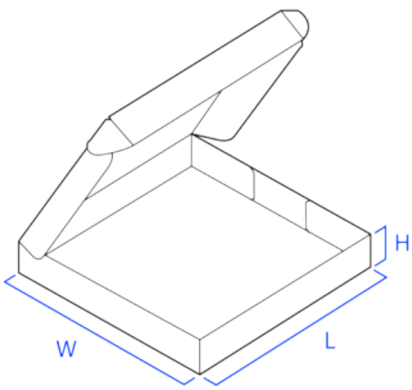
Note: Wo and Wi measured at hub



Dimensions (mm)

	Nominal	Tolerance
P1	8.00	+/- 0.1
W	12.00	+ 0.3 / - 0.1
Ko	0.83	+/- 0.1
Ao	4.67	+/- 0.05
Bo	4.80	+/- 0.05
Sp	4.00	+/- 0.02
Sd	1.50	+ 0.1 / - 0.0
St	1.75	+/- 0.1
SA	5.50	+/- 0.05
SB	2.00	+/- 0.05

Tape and Reel Box Dimensions



Outside dimensions (mm)

	7" mini-reel	13" tape-reel
W	197	342
L	204	355
H	32	53